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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,198	03/11/2004	Toshiyuki Koimori	SON-2950	4731

23353 7590 07/13/2005

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EXAMINER	
NGUYEN, HIEU P	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,198	KOIMORI ET AL.	
	Examiner	Art Unit	
	Hieu Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/11/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 5 objected to because of the following informalities:

Claim 5, line 1, a colon should be used instead of a semicolon.

Claim 5, line 21, a comma should be used instead of a period.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama et al. (US 6329879) view of Ariyoshi (US 5659264).

Regarding claim 1, Fig. 21 of Maruyama shows a power amplifier comprising: a field effect transistor (7), a bias voltage supply terminal (5) supplied with a bias voltage (Vgg), a reference potential (6), a first resistance element (16), and a second resistance element (15). A first terminal of the first resistance element and a first terminal of the second resistance element are connected and the connection point of those terminals is connected to a gate terminal (G) of the field effect transistor, a second terminal of the

first resistance element is connected to the bias voltage supply terminal, a second terminal of the second resistance element is connected to the reference potential.

Maruyama fails to disclose "a second resistance element with a temperature coefficient smaller than that of the first resistance element". However, Ariyoshi discloses [column 5, lines 33-46; Fig. 1] a reference voltage circuit constituted by a voltage follower wherein a divided voltage 9 (ND1) established by resistors r1 (first resistance element), R6 and R5 (second resistance element) with temperature coefficient smaller than that of the first resistance element in the case where the temperature drift in the output voltage of the amplifier circuit has a positive coefficient.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Ariyoshi into the circuit of Maruyama by having second resistance element with a temperature coefficient smaller than that of the first resistance element. The ordinary artisan would have been motivated to modify in the manner set forth above for at least the purpose of controlling the temperature drift.

Maruyama discloses the field effect transistor and the second resistance element (Fig.21, R1 (15)) are semiconductor devices formed on the same semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the field effect transistor and either first or second or both resistance elements formed on the same semiconductor substrate. The ordinary artisan would have been motivated to modify in the manner set forth above for at least the purpose of reducing in size of the power amplifier system.

Regarding claims 2,4 and 6, Maruyama discloses [column 4, line17-20] one resistor of the resistance type potential divider circuit is comprised of a temperature-compensating resistor whose resistance value varies linearly. Fig. 21 of Maruyama shows the temperature-compensating resistor (15) is connected to the ground (6).

Regarding claim 3, Fig. 21 of Maruyama shows a power amplifier comprising: a field effect transistor (7), a bias voltage supply terminal (5) supplied with a bias voltage (Vgg), a reference potential (6), a first resistance element (16), a second resistance element (15), wherein a first terminal of the first resistance element and a first terminal of the second resistance element are connected and the connection point of those terminals (G) is connected to a gate terminal of the field effect transistor (7), a second terminal of the first resistance element (16) is connected to the bias voltage supply terminal (5).

Maruyama discloses the field effect transistor and the second resistance element (Fig.21, R1 (15)) are semiconductor devices formed on the same semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the field effect transistor and either first or second or both resistance elements formed on the same semiconductor substrate. The ordinary artisan would have been motivated to modify in the manner set forth above for at least the purpose of reducing in size of the power amplifier system.

Maruyama shows most aspects of the instant invention except: " a third resistance element with a temperature coefficient smaller than those of the first resistance element and the second resistance element ". However, Ariyoshi discloses

[column 5, lines 33-46; Fig. 7] a reference voltage circuit constituted by a voltage follower wherein a third resistance element (r1) with a temperature coefficient smaller than those of the first resistance element (R5), and the second resistance element (R6) in the case where the temperature drift in the output voltage of the amplifier circuit has a positive coefficient, a second terminal of the second resistance element is connected to the first terminal of the third resistance element, a second terminal of the third resistance element is connected to the reference voltage, and the field effect transistor.

It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Ariyoshi into the circuit of Maruyama by having a variable second resistance element. The ordinary artisan would have been motivated to modify in the manner set forth above for at least the purpose of controlling the temperature drift.

Regarding claim 5, Fig. 21 of Maruyama shows a power amplifier comprising: a field effect transistor (7), a bias voltage supply terminal (5) supplied with a bias voltage (Vgg), a reference potential (6), a first resistance element (16), a second resistance element (15), wherein a first terminal of the first resistance element and a first terminal of the second resistance element are connected, a second terminal of the first resistance element is connected to the bias voltage supply terminal.

Maruyama discloses the field effect transistor and the second resistance element (Fig.21, R1 (15)) are semiconductor devices formed on the same semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the field effect transistor and either first or

second or both resistance elements formed on the same semiconductor substrate. The ordinary artisan would have been motivated to modify in the manner set forth above for at least the purpose of reducing in size of the power amplifier system.

Maruyama shows the most aspect of the instant invention except "a second resistance with a temperature coefficient smaller than that of the first resistance element, and a third resistance element with a temperature coefficient smaller than that of the first resistance element, wherein a second terminal of the second resistance element and a first terminal of the third resistance element are connected, a connection point of those terminals is connected to a gate terminal of the field effect transistor".

However, Ariyoshi discloses [column 5, lines 33-46; Fig. 8] a reference voltage circuit constituted by a voltage follower wherein a first resistance element (r1), a second resistance (R5) with a temperature coefficient smaller than that of the first resistance element, and a third resistance element (R6) with a temperature coefficient smaller than that of the first resistance element in the case where the temperature drift in the output voltage of the amplifier circuit has a positive coefficient, wherein a second resistance element and a first terminal of the third resistance element are connected, a connection point of those terminals is connected to a gate terminal of the field effect transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 703-861-9326. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hn

ZANDRA V. SMITH
PRIMARY EXAMINER